Research on Image Acquisition and Processing System based on FPGA

Haoyan Hu

Xiangtan University, China

Keywords: High Resolution; High Frame Rate; FPGA.

Abstract: This paper presents a hardware scheme of high-speed image acquisition and processing system based on FPGA. The working principle of high-speed and high-resolution image acquisition system is discussed. The system design is completed based on the researches on burst data temporary storage, large capacity data transfer, high resolution, high frame rate image real-time transmission and large capacity data terminal transmission. The test results of the hardware circuit show that the system can collect and store the high-speed and large-capacity data stream generated by the image sensor. The high-speed image acquisition system designed with the core processor of FPGA greatly simplifies the hardware structure of the system and improves the reliability of the system.

1. Introduction

With the continuous development of society, image acquisition and processing technology play a crucial role in many industries, such as military, security monitoring, industrial vision and other fields, and the requirements for image acquisition and processing technology in all walks of life are also increasingly high. High-speed and real-time transmission is one of the main development trends. Image acquisition is the basis of image processing. As the frame rate and resolution of image acquisition become higher and higher, the requirement of high-speed image processing and display is also growing.

High-speed camera (generally referred to as frame rate above 100 frames/s) has a wide range of applications in the military field [1]. In the high-speed image acquisition system, the receiver receives a large amount of data instantaneously. To process and analyze such a large amount of burst data, image data must be collected by high-speed camera. Because of the huge amount of data in the high-resolution image processing system, the real-time processing speed of hardware processor requires to be very high. It is necessary to reasonably design a hardware circuit to meet the requirements of system resolution and image frame rate. Most high-speed cameras use the Camera Link interface, and the data transmission rate of Full Camera Link camera can reach 680 MB/s. Thus, how to design and implement a high-speed image processing platform is of great significance.

Most of the platforms for image processing send the collected images to PC through PCI or USB interface for further image processing and displaying. The system is large in size and high in cost, which is limited by the processing speed of PC, and the real-time performance of image display will be affected. A few embedded platforms do not process the original images but simply display them directly. Accordingly, the quality of the displayed images is influenced. Moreover, these platforms employ Small capacity SDRA to cache the data, which cannot be applied to image processing with a large amount of data.

At present, the advancement of video image acquisition and processing technology is mainly divided into two categories. One is to process video image by software based on PC on specific PCIe acquisition board; the other is to collect and process video image by related integrated hardware such as DSP, MCU and FPGA. Relatively speaking, the processing effect of the latter is not as good as that of the former, but it has better real-time performance, small volume and convenient use, and is more suitable for industrial needs.

The field programmable logic gate array (FPGA)adopts a parallel operation mode and has a high working frequency. It can operate and process a large amount of data in real time, with an obvious advantage in the field of communication and image processing.

Therefore, this paper designs a high-speed image acquisition, processing and display platform based on FPGA. The acquired image is buffered by frame in the large capacity memory chip DDR2SDRAM by the FPGA, and each frame of image is read out from the DDR2 for preprocessing. The image is processed by the complex algorithm by the DSP. Finally, the image is sent to the DVI encoding chip by the FPGA for display. The speed of image processing is fast and the real-time display is sound. The platform has the merits of small size, low cost, a large amount of data processing, fast processing speed and wide applicability.

This paper designs the system from the following aspects: temporary storage of burst data, large capacity data transfer, real-time transmission of high resolution and high frame rate images, and terminal transmission and display of large capacity data.

2. Working Principle of High Resolution and High-Speed Image Acquisition System

The block diagram of high resolution and high-speed image acquisition system principle is shown in Fig. 1. It consists of an image sensor, FPGA, DDRS2 DRAM, Flash memory, FRAM, LVDS, embedded motherboard, Ethernet and other modules. The high-speed camera system rotates at a predetermined angular speed and compresses the searched flying target image to CMOS image sensor. The CMOS sensor converts photoelectric signals into analog electrical signals, which are then converted into analog-to-digital (AD) signals and sent to the internal of the FPGA for processing. The driver module of the CMOS image sensor is built in the FPGA to generate the driving signal needed by CMOS. Part of these digital image data are transmitted to DDRS2 DRAM memory for temporary storage through the control of FPGA, and then sent to PC through embedded motherboard for further processing and data analysis. The other image data are synthesized into VGA signal, and the real-time signal is transmitted to monitor by means of LVDS differential transmission.

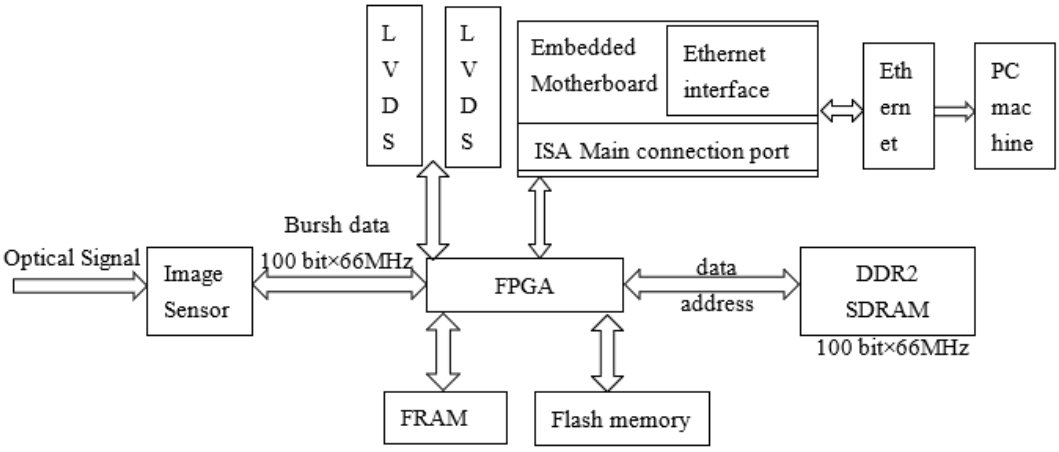

Fig.1 Principle Diagram of high-speed image acquisition system

3. Design of High Resolution and High-Speed Image Acquisition System

3.1 Temporary Storage of Burst Data

The moving image information of the target enters the image sensor through the optical system. The analog-to-digital converter (ADC) in the image sensor chip converts the analog signal into the digital signal and transmits it to the control unit of the FPGA. As the image sensor outputs 10 channels of 10 bits wide data and the clock frequency is 66 MHz, it will generate 100 bits × 66 MHz (about 0.825 GB/s) of data. Such a fast amount of data i.e. burst data stream, cannot be directly

stored on the hard disk. It needs to be temporarily stored in the memory bar (DDR2 SDRAM). DDRS2 DRAM memory is accessed by FPGA to control the timing operation of reading, writing and refreshing burst data with large capacity.

The connection block diagram of DDR2 SDRAM and FPGA is shown in Figure 2. DDR2 SDRAM is a kind of high-speed dynamic random-access memory with the synchronous interface. This synchronous interface and its internal Pipeline structure render it a very high data transmission rate. DDRS DRAM adopts a multi-block bank memory structure and burst mode, and each bank is addressed by rows and columns, where column address space corresponds to one page of memory space.

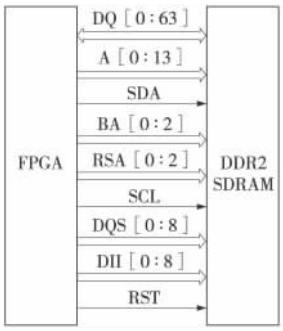

Fig.2 Protocol of DDR2, SDRAM and FPGA interface

Considering the need for which high-speed image acquisition system to support 1GB or even 4GB capacity, DDRS2 DRAM is chosen as memory in this paper. DDRS 2 DRAM is a replacement product of DDRS DRAM [2]. Its memory structure is similar to DDR SDRAM. The biggest change is that it introduces 4-bit data prefetch architecture to improve memory frequency and enhance the parallel operation ability of memory cells [3]. The same transmission rate being provided and meanwhile the operating frequency of the storage unit being reduced, the bandwidth provided by the whole memory module is finally improved [4].

3.2 Design of Large Capacity Data Transfer

Since DDRS2 DRAM loses all data once it loses power, it is necessary to forward large-capacity data stored in DDRS2 DRAM to memory that can store the data permanently. In this paper, large capacity data transfer technology is adopted to realize the permanent storage of data in DDRS2 DRAM.

In this paper, we choose Flash which can maintain data once power is off and can erase and programme to store large capacity data once power is on. Flash chips with 1 GB/chip x 4 chip super-large capacity and non-NAND structure are used to receive and forward image data. Flash with NAND structure has the large capacity, fast write-back speed and small chip area, while NAND structure can provide very high cell density, and high-speed writing and erasing ability, which is suitable for high-density data storage.

The design principles of large capacity data transfer are as follows. When the image data acquisition is completed, the write operation of DDRS2 DRAM is stopped, and the FPGA controls DDRS2 DRAM to transfer the image data into Flash. As DDRS2 DRAM has a very high speed and Flash is a low-speed asynchronous memory, the synchronization of data transmission between them should be taken into consideration in the design of image data transfer system. Hence, during the transfer operation, the FPGA can detect all through whether the data read from DDRS2 DRAM in the current cycle is stored in Flash. If the storage is not completed, the DDRS2 DRAM cannot stop reading data until the current data is stored in Flash, and the data read in the next cycle of DDRS2 DRAM cannot be carried out.

3.3 Design of Real-time Transmission of High Resolution and High Frame Frequency Images

In order to ensure the synchronization of data acquisition and image processing, it is necessary to transfer the collected and stored high-speed and high-resolution images to the follower rack of the

high-speed camera system in real time. In this paper, low voltage differential signaling (LVDS) is adopted to transmit image data in real time. LVDS is a low swing differential signal technology, which uses a pair of differential lines to achieve high-speed signal transmission, so that the signal can be transmitted at hundreds of MB/s on differential PCB line pairs or balanced cables. The LVDS has the advantages of low noise and low power consumption [5].

The image data needed to be transmitted by the high-speed camera system is 1280 x 1024 and the frame rate is 500 Hz. For the sake of real-time transmission, the data needed to be transmitted are as follows:

$$1280\times1024\times500=655.36,\text{MB/s}. \tag{1}$$

Assuming that the selected LVDS is a 28 bit channel link 66MHz chip with a bit width of 28 bits, which can transmit about 3B at a time, the data can be transmitted as follows:

$$3\times66=198,\text{MB/s}. \tag{2}$$

Using multiple LVDS chips to transmit in parallel, the number of chips needed is

$$655.36/198=3.31. \tag{3}$$

Therefore, four LVDS chips should be selected for parallel output.

3.4 Large Capacity Data Terminal Transmission and Display

To facilitate the subsequent processing of the acquired image data by user terminals, the FPGA connects with the embedded motherboard through ISA bus interface. It transmits the data in the specified address segment of memory bar to the user PC via the Ethernet interface of the embedded system until the burst process and the transfer operation is finished.

For the purpose of transmitting large-capacity data, 100-megabit Ethernet is selected. Hundred Megabit Ethernet is a new high-speed LAN based on standard Ethernet, which can provide 100 Mbit/s communication bandwidth, especially suitable for high-speed and large-capacity data transmission in this design.

Since the maximum resolution of the CMOS image sensor can reach 1280×1024, it is much higher than the maximum resolution of the ordinary TV video signal. In order to display the processed image, a computer monitor with VGA interface must be used. Computer display has become a common output device in most designs because of its large amount of output information and various output forms. The display adopts progressive scanning to display [6].

4. Simulation Results

In high-speed image acquisition system, FPGA is the core control device, which controls all peripheral chips. It has the characteristics of high density, high speed, high bandwidth and strong versatility, which is very suitable for the design requirements of high-speed system [7]. The selection of FPGA mainly takes into accounts the size of the chip (RAM size, number of logical units, etc.), the number of users' I/O and level compatibility. According to the design requirements, we choose the Stratix II series of FPGA of Altera Company, which uses advanced design framework, including adaptive logic module (ALM), logic array block (LAB), TriMatrix memory, external memory interface and digital signal processing (DSP) module.

In this paper, the hardware description language is employed to realize the logic design and control of the image acquisition system by the FPGA. Fig. 3 is the simulation results of several time series intercepted, and Fig. 4 is the frame time sequence of the sensor.

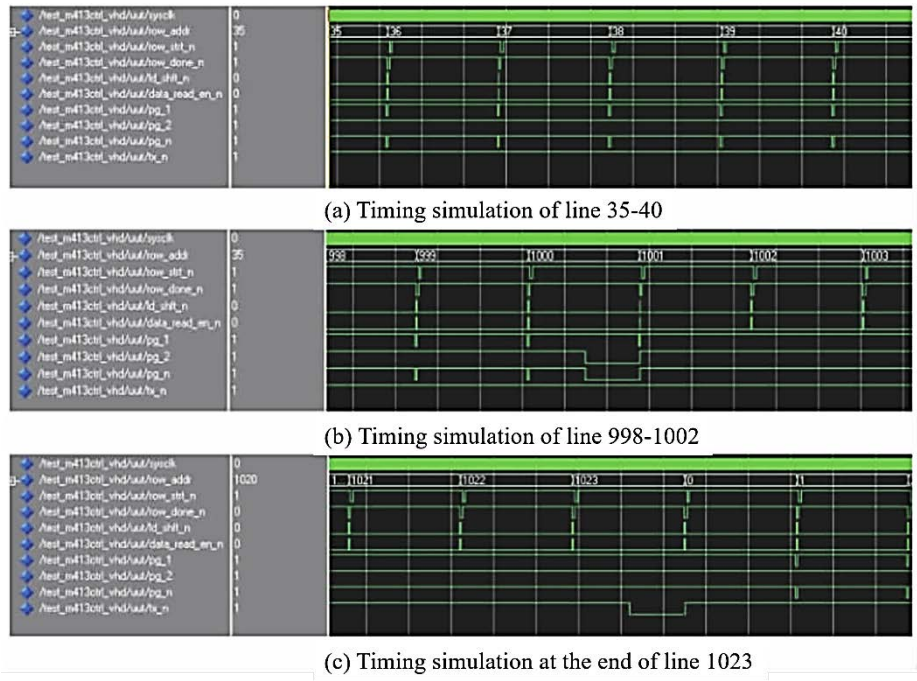

Fig.3 Simulation result

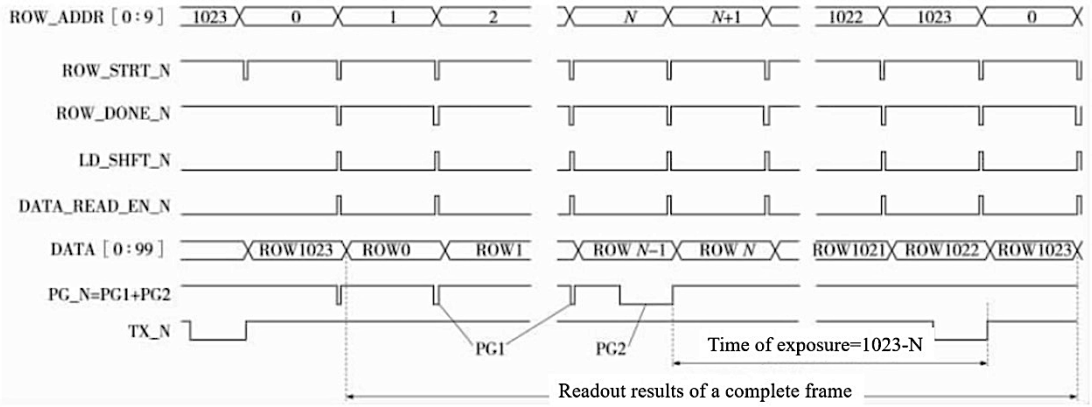

Fig.4 Frame timing sequence of the sensor

Compared with Figures 3 and 4, it can be seen that the simulation results are consistent with the timing results in the sensor.

5. Conclusion

Based on the core control device of FPGA, the author designs a high-speed image acquisition system from the perspectives of burst data temporary storage, large capacity data transfer, real-time transmission of high resolution and high frame rate images, large capacity data terminal transmission and display. It is demonstrated that the acquisition system can process, transmit and display instantaneous burst data in real time when the requirement of frame rate and resolution is relatively high, satisfying the design requirements.

References

[1] Yang Huiling, WangJun, YangHuiwei. Design of high frame frequency CMOS real-time image acquisition system [J]. Microcomputer Information,2008,24 (3): 309-311.

[2] Chen Guozhu, LiuTao, LiYuanzong. Design of image sampling and storage system based on FPGA[J]. Mechanical Engineering & Automation,2007(4):44-46.

[3] Stuart K. High-speed, high-sensitivity, low-noise scientific CMOS image sensors [J]. Proceedings of SPIE,2004,5274:194-205.

[4] Wang Jianhua, Liu Chanlao, Chen Dachuan, et al. Design of real-time video processing system based on DSP+FPGA[J]. Foreign Electronic Measurement Technology,2007,26(9):42-44,48.

[5] HuangJin, Guo Lihong, Li Yan, et al. High-speed CCD digital video acquisition and parallel storing technology[J]. Journal of Changchun University of Science and Technology,2004,27(3):104-106.

[6] Geng Yubo, Zhang Xiaodong, Chen Xi. A high-speed real-time data acquisition system based on PCI bus[J]. Industrial Control Computer,2005,18(5):32-33.

[7] Xu Wanying, Liu Jianjun, Huang Xinsheng. Study on high-speed image acquisition technology based on CPLD and DSP[J]. Electronic Engineer,2004,30(6):48-50.